WE CLAIM:

1. A method for reducing the drain resistance of a drain-extended MOS transistor in a semiconductor wafer, while maintaining a high transistor breakdown voltage, comprising the steps of:

providing a first well of a first conductivity type, operable as the extension of the transistor drain of said first conductivity type and covered by a first insulator having a first thickness, and a second well of the opposite conductivity type, intended to contain the transistor source of said first conductivity type and covered by a second insulator thinner than said first insulator, said first and second wells forming a junction that terminates at said second insulator;

depositing a photoresist layer over said wafer;

patterning said photoresist layer by opening a window laterally extending from said drain to said junction termination; and

implanting ions of said first conductivity type through said window into said first well, said ions having an energy to limit the penetration depth to said first insulator thickness, and a dose to create a well region of high doping concentration adjacent to said junction termination.

2. The method according to Claim 1 wherein said first insulator thickness is in the range from 450 to 600 nm.

3. The method according to Claim 1 wherein said second insulator is less than 50 nm thick.

4. The method according to Claim 3 wherein said second

insulator thickness is in the range from 1 to 15 nm.

5. The method according to Claim 1 wherein said first conductivity type is p-type and said opposite conductivity type is n-type.

6. The method according to Claim 5 wherein said implanted ions of the first conductivity type are boron ions.

7. The method according to Claim 6 wherein said boron ions have an energy of about 15 to 25 keV and a dose in the approximate range from 2 to 6E11/cm^2.

8. The method according to Claim 1 wherein said first conductivity type is n-type and said opposite conductivity type is p-type.

9. The method according to Claim 8 wherein said implanted ions of the first conductivity type are phosphorus ions.

10. The method according to Claim 9 wherein said phosphorus ions have an energy of about 40 to 60 keV and a dose in the approximate range from 1 to 3E12/cm^2.

11. A method for fabricating, on the surface of a semiconductor wafer of a first conductivity type, an MOS transistor having a channel of said first conductivity type, comprising the steps of:

forming a buried layer of the opposite conductivity type in said wafer, said buried layer separating the region, in which said transistor is to be fabricated, from the remainder of said wafer;

forming a first well of the opposite conductivity type, said first well having a sidewall;

forming a second well of said first conductivity type and low doping concentration, said second well having a sidewall so that a junction is formed with said sidewall of said first well,

said junction terminating at the surface of said wafer;

forming a first insulator layer over portions of said first and second wells;

forming a second insulator layer over the remainder of said first and second wells, said second insulator layer thinner than said first insulator layer, said second insulator layer protecting said junction termination;

depositing a photoresist layer over said wafer;

patterning said photoresist layer by opening a window approximately as wide as said second well, including said junction termination;

implanting ions of said first conductivity type through said window into said second well, said ions having an energy limiting the penetration to said thickness of said second insulator layer, and a dose to create a region in said second well having higher doping concentration than the remainder of said well, said region adjacent to said junction termination;

removing said photoresist layer;

removing said second insulator layer;

forming the insulator layer for said gate over said first well, and completing said gate;

forming the polysilicon layer; and

forming said source in said first well and concurrently said drain in said second well.

12. The method according to Claim 11 wherein said first insulator thickness is in the range from 450 to 600 nm.

13. The method according to Claim 11 wherein said second insulator thickness is less than 50 nm.

14. The method according to Claim 13 wherein said second insulator thickness is in the range from 1 to 15 nm.

15. The method according to Claim 11 wherein said first conductivity type is p-type and said opposite conductivity type is n-type.

16. The method according to Claim 11 wherein said implanted ions of the first conductivity type are boron ions.

17. The method according to Claim 16 wherein said boron ions have an energy of about 15 to 25 keV and a dose in the approximate range from 2 to 6E11/cm^2.

18. The method according to Claim 11 further comprising the step of depositing a layer of epitaxial, low-doping-concentration semiconductor material of said first conductivity type after said step of forming said buried layer, before said steps of forming said wells.

19. A method for fabricating, on the surface of a semiconductor wafer of a first conductivity type, an MOS transistor having a channel of the opposite conductivity type, comprising the steps of:

forming a first well of the opposite conductivity type, said first well having a sidewall;

forming a second well of said first conductivity type, said second well having a sidewall so that a junction is formed with said sidewall of said first well, said junction terminating at the surface of said wafer;

forming a first insulator layer over portions of said first and second wells;

forming a second insulator layer over the remainder of said first and second wells, said second insulator layer thinner than said first insulator layer, said second insulator layer protecting

said junction termination;

depositing a photoresist layer over said wafer;

patterning said photoresist layer by opening a window approximately as wide as said first well, including said junction termination;

implanting ions of said opposite conductivity type through said window into said first well, said ions having an energy limiting the penetration to said thickness of said second insulator layer, and a dose to create a region in said first well having higher doping concentration than the remainder of said well, said region adjacent to said junction termination;

removing said photoresist layer;

removing said second insulator layer;

forming the insulator layer for said gate over said second well and completing said gate;

forming the polysilicon layer; and

forming said source in said second well and concurrently said drain in said first well.

20. The method according to Claim 19 wherein said first insulator thickness is in the range from 450 to 600 nm.

21. The method according to Claim 19 wherein said second insulator thickness is less than 50 nm.

22. The method according to Claim 21 wherein said second insulator thickness is in the range from 1 to 15 nm.

23. The method according to Claim 19 wherein said first conductivity type is p-type and said opposite conductivity type is n-type.

24. The method according to Claim 19 wherein said implanted ions of the opposite conductivity type are phosphorus ions.

25. The method according to Claim 24 wherein said phosphorus ions have an energy of about 40 to 60 keV and a dose in the approximate range from 1 to 3E12/cm^2.